CV date: 2024-10-16

Part A. PERSONAL INFORMATION

First and Family name		Jesús Lázaro Arrotegui
ID# —	Age	—
Researcher codes	ResearchID	K-2666-2017
	Código Orcid	0000-0002-7483-3609

A.1. Current position

Name of University/Institution	Universidad del País Vasco/Euskal Herriko Unibertsitatea		
Department	Escuela de Ingeniería de Bilbao, Dept. Tecnología Electrónica		
Address and Country	Plaza Ingeniero Torres Quevedo, 1. 48013 Bilbao. Spain		
Phone number	946017344	E-mail	jesus.lazaro@ehu.eus
Current position	Full professor	From	2019-02-02
UNESCO code	330700		
Key words	FPGA,SoC		

A.2. Education

PhD, Licensed, Graduate	University	Year
Telecommunication engineer	E.T.S. Ingeniería, Bilbao	2001
PhD Telecommunication engineer	E.T.S. Ingeniería, Bilbao	2005

A.3. General indicators of quality of scientific production

1. Research six-year periods:
   a) 2014-01-01 - 2019-12-31
   b) 2008-01-01 - 2013-12-31
   c) 2002-01-01 - 2007-12-31
2. Q1/Q2 publications since last six year research period (2019):
   - AXI Lite redundant on-chip bus interconnect for high reliability systems. IEEE Transactions on Reliability (2024-04-01) IF: 5.000 Q1
   - High performance platform to detect faults in the Smart Grid by Artificial Intelligence inference. IEEE Transactions on Smart Grid (2024-01-01) IF: 8.600 Q1
   - Encryption AXI transactions core for enhanced FPGA security. Electronics (2022-10-18) IF: 2.900 Q2
   - Specific electronic platform to test the influence of hypervisors on the performance of embedded systems. technologies (2022-04-22) IF: 3.600 Q1
   - Time Sensitive Networking protocol implementation for Linux end equipment. technologies (2022-04-22) IF: 3.600 Q1
   - Embedded firewall for on-chip bus transactions. Computers and Electrical Engineering (2022-03-01) IF: 4.300 Q2
   - High-performance computing architecture for Sample Value processing in the Smart Grid. IEEE Access (2022-01-24) IF: 3.900 Q2
   - Fast and efficient address search in System-on-a-Programmable-Chip using binary trees. Computers and Electrical Engineering (2021-12-01) IF: 4.152 Q2
   - A Survey on Vulnerabilities and Countermeasures in the Communications of the Smart Grid. Electronics (2021-08-31) IF: 2.690 Q2
   - A Fixed-Latency Architecture to Secure GOOSE and Sampled Value Messages in Substation Systems. IEEE Access (2021-04-30) IF: 3.476 Q2

Parte B. CURRICULUM

Since my entry as associate professor at the end of 2001 at the University of the Basque Country/Euskal Herriko Unibertsitatea, I have followed an intense research work that has been rewarded with 3 positive evaluation of six-year research periods. I am a member of the Apert research group since its foundation in 2002. During these years the members of the group have managed to turn the Apert research group into a recognized group as evidenced by the general group grants it has enjoyed and continues to enjoy, the latter as a consolidated group of the Basque Government and as a member of the Training and Research Unit in Telecommunications and Electronics of the Basque Government. During these years I have participated in 56 public projects that have resulted in 46 contributions in journals and 81 in congresses in the area of reconfigurable circuits. My research career has led me to realize high performance circuits for high speed communications. In recent years, my knowledge in FPGA internal structures has led me to be interested in fault-tolerant circuits. It is worth mentioning in this aspect my stay at VT with Professor Athanas, one of the leading experts in the area.

During these years I have achieved multiple accreditations highlighting that of assistant professor (ANECA). I have 4 Five-year teaching periods as well as complements (UNIBASQ).

The research work has been combined with my teaching work in multiple specialized courses for companies, teaching in doctoral and master's degree programs.

In my eagerness to transfer the knowledge generated at the University to the business fabric of my environment, I am co-author of 4 patents and I have participated in more than Research Projects with private funding. As a highlight in this transfer, I am a founding partner of the company System-on-Chip engineering. This company, created in 2010, employs, as of today, 14 alumni of the School of Engineering of Bilbao and is dedicated to the design of IP cores in the field of industrial communications.

Since 2019 I am a full professor of the electronic technology department. At the same time I am a member of the UPV/EHU university teaching staff statutory commission, member of the Basque language commission and of the academic planning commission of the School of Engineering of Bilbao and member of the PhD program commission in Electronics and Telecommunications.

Part C.RELEVANT MERITS

C.1. Publications

1. AXI Lite redundant on-chip bus interconnect for high reliability systems. IEEE Transactions on Reliability (2024-04-01) IF: 5.000 Q1

2. High performance platform to detect faults in the Smart Grid by Artificial Intelligence inference. IEEE Transactions on Smart Grid (2024-01-01) IF: 8.600 Q1

3. Encryption AXI transactions core for enhanced FPGA security. Electronics (2022-10-18) IF: 2.900 Q2

4. Specific electronic platform to test the influence of hypervisors on the performance of embedded systems. technologies (2022-04-22) IF: 3.600 Q1

5. Time Sensitive Networking protocol implementation for Linux end equipment. technologies (2022-04-22) IF: 3.600 Q1

6. Embedded firewall for on-chip bus transactions. Computers and Electrical Engineering (2022-03-01) IF: 4.300 Q2

7. High-performance computing architecture for Sample Value processing in the Smart Grid. IEEE Access (2022-01-24) IF: 3.900 Q2

8. Fast and efficient address search in System-on-a-Programmable-Chip using binary trees. Computers and Electrical Engineering (2021-12-01) IF: 4.152 Q2

9. A Survey on Vulnerabilities and Countermeasures in the Communications of the Smart Grid. Electronics (2021-08-31) IF: 2.690 Q2

10. Evaluating Latency in Multiprocessing Embedded Systems for the Smart Grid. Energies (2021-06-30) IF: 3.252 Q3

C.2. Research projects

1. Investigación y capacitación del ecosistema I+D+I en el diseño, fabricación y testing de semiconductores para sistemas críticos. Eusko Jaurlaritza/Gobierno Vasco 2023-03-03 → 2024-12-31 219,333.32 € IP: A. Astarloa
2. Infraestructura experimental mejorada para investigación en 5G y 6G y servicios avanzados sn4e+ (enhanced smart networks for everything). Ministerio de Asuntos Económicos y Transformación Digital 2023-10-01 → 2025-06-30 1,975,632.00 € IP: E. Taquet
3. Grupo de Investigación en Electrónica Aplicada (APERT). Grupo A. IT1440-22.. Gobierno Vasco (Ayudas para apoyar las actividades de grupos de investigación del sistema universitario vasco) 2022-01-01 → 2025-12-31 395,000.00 € IP: J.L. Martín
4. Analizador de señal y espectro. Universidad del País Vasco (UPV/EHU) 2022-01-01 → 2022-12-31 4,803.00 € IP: **J. Lázaro**
5. Infraestructura experimental para investigación en 5G y 6G y servicios avanzados SN4E (Smart networks for everything). Ministerio de Asuntos Económicos y Transformación Digital 2022-09-07 → 2025-06-30 1,999,274.00 € IP: E. Taquet
6. Itsas energiarentzako urpekari autonomoen diseinu taldea, grupo de diseño de vehiculos submarinos autonomos para energías marinas, AUUV design group. Universidad del País Vasco (UPV/EHU) 2021-12-15 → 2022-12-31 5,000.00 € IP: I. Mtnez. De Alegría
7. XXXIV Conference on Design of Circuits and Integrated Systems. Universidad del País Vasco (UPV/EHU) 2020-04-20 → 2020-04-21 2,400.00 € IP: J. Jiménez
8. Tecnología Electrónica. Universidad del País Vasco (UPV/EHU) 2020-01-01 → 2023-12-31 14,054.01 € IP: **J. Lázaro**
9. Osciloscopio digital RTP de gran ancho de banda. Universidad del País Vasco (UPV/EHU) 2020-01-01 → 2020-12-31 23,018.00 € IP: J. Jiménez
10. XXXIV Conference on Design of Circuits and Integrated Systems. Eusko Jaurlaritza/Gobierno Vasco 2019-11-22 → 2020-05-22 10,000.00 € IP: A. Zuloaga

C.3. Contracts, technological or transfer merits

1. AEROSECURE: switch/router ciberseguro para aplicaciones aerotransportadas de tiempo real. System-on-Chip engineering S.L. 2024-05-06 → 2026-12-30 49,940.00 € IP:
2. Análisis y aplicación de la tecnología 5g en vehículos aéreos no tripulados (UAV) para aplicaciones de vigilancia, reconocimiento y soporte a la gestión de emergencias - AERO 5. System-on-Chip engineering S.L. 2024-09-03 → 2025-12-31 149,600.00 € IP: A. Astarloa
3. Informe técnino sobre estructura RF datalogger. Artic SEA, S.L. 2023-02-14 → 2023-05-13 3,500.00 € IP: **J. Lázaro**
4. Plataforma de testeo para la automatización, protección y control de procesos en las subestaciones eléctricas - PAPOS. System-on-Chip engineering S.L. 2023-05-08 → 2024-12-31 75,000.00 € IP: A. Astarloa
5. TSNAero: Diseño y desarrollo de tecnología y producto electrónico certificable para comunicación ethernet determinista (TSN) en plataformas del sector aviónica y aerospacio. System-on-Chip engineering S.L. 2022-05-02 → 2024-12-30 118,000.00 € IP: A. Astarloa
6. COMMUTE: Plataforma de comunicaciones ethernet de altas prestaciones, cibersegura, orientada a aplicaciones críticas, y reconfigurable. PT10729. System-on-Chip engineering S.L. 2021-05-03 → 2023-07-31 50,000.00 € IP: A. Astarloa
7. TOPIC: Análisis de protocolos serie para intercambio de datos con requisitios estrictos de tiempo real. PT10724. Ingeteam Power Technology S.A. 2021-11-15 → 2022-03-14 9,750.00 € IP: A. Astarloa
8. Apoyo técnico a proyecto HAZITEK IKERTU II. Jema Energy S.A. 2021-12-15 → 2024-12-15 246,161.00 € IP: I. Mtnez. De Alegría

9. Computación distribuida e interoperable para una inteligencia artificial en tiempo real en smart factories (PILAR). System-on-Chip engineering S.L. 2020-05-07 → 2022-10-15 332,320.00 € IP: J. Jiménez

10. Collaboration in the Study of Power Converter Topologies for Inner Triplet magnets with Energy Recovery in the framework of the High Luminosity upgrade for the LHC at CERN. CERN/APERT (UPV/EHU) 2019-12-02 → 2022-08-31 135,000.00 € IP: I. Mtnez. De Alegría

C.4. Patents

1. J. Lázaro, A. Astarloa y M. Idirin. Método y sistema de seguridad en anillos ethernet redundantes. P201530970. ES2596533. España. 2017-01-10. UPV/EHU & SoC-e.

2. J.A. Araujo, J. Lázaro, A. Astarloa y A. Zuloaga. Sistema y método de lectura y escritura de una memoria digital. P201430599. ES2549188. España. 2016-05-19. UPV/EHU.

3. J. Lázaro, A. Astarloa, U. Bidarte y A. Zuloaga. Votador aritmético por mayoría. P201031492. ES2379239B1. España. 2012-04-24. UPV/EHU.

4. U. Bidarte, A. Astarloa, J. Lázaro y A. Zuloaga. Generador de números realmente aleatorios. P200702299. ES200702299. España. 2010-10-16. UPV/EHU.

C.5. Conferences

1. A. Astarloa, P. Fernández, J. Lázaro, M. Idirin, S. Salas. Time-Sensitive Networking to meet Hard-real Time Boundaries on Edge Intelligence Applications. DCIS 2023. Málaga. 2023-11-15 → 2023-11-17.

2. S. Alonso, J. Lázaro, J. Jiménez, L. Muguira, U. Bidarte. Timing requirements on multi-processing and reconfigurable embedded systems with multiple environments. DCIS 2023. Málaga. 2023-11-15 → 2023-11-17.

3. JL. Unibaso, JA. Araujo, J. Lázaro, J. Jiménez, L. Muguira. Design and development of an IoT device provided with a voice interface to improve treatment adherence in polymedicated patients. DCIS 2022. Pamplona. 2022-11-16 → 2022-11-18.

4. A. Santiago, L. Muguira, J. Jiménez, L. Sun, J. Lázaro. Analysis and Deployment of Applications Acceleration Environment for Xilinx Hardware-Accelerated Platforms. DCIS 2022. Pamplona. 2022-11-16 → 2022-11-18.

5. S. Alonso, J. Lázaro, J. Jiménez, L. Muguira, U. Bidarte. The influence of virtualization on real-time systems' interrupts in embedded SoC platforms. DCIS 2022. Pamplona. 2022-11-16 → 2022-11-18.

6. S. Alonso, J. Lázaro, J. Jiménez, L. Muguira, U. Bidarte. Evaluating the OpenAMP framework in real-time embedded SoC platforms. DCIS 2021. Oporto (Portugal). 2021-11-24 → 2021-11-26.

7. L. Muguira, J. Lázaro, S. Alonso, A. Astarloa, M. Rodríguez. Secure Critical Traffic of the Electric Sector over Time-Sensitive Networking. DCIS 2020. Segovia. 2020-11-18 → 2020-11-20.

8. A. Astarloa, M. Rodríguez, F. Durán, J. Jiménez, J. Lázaro. Synchronizing NTP Referenced SCADA Systems Interconnected by High-availability Networks. DCIS 2020. Segovia. 2020-11-18 → 2020-11-20.

9. S. Alonso, J. Lázaro, J. Jiménez, L. Muguira, A. Largacha. Analysing the interference of Xen hypervisor in the network speed. DCIS 2020. Segovia. 2020-11-18 → 2020-11-20.

10. J. Lázaro, L. Burgos, L. Muguira, A. Astarloa, J. Jiménez. Electronic control board for student Rocket. DCIS 2020. Segovia. 2020-11-18 → 2020-11-20.

C.6, International stays

1. Virginia Technology. Blacksburg VA (USA) 2010 (11 weeks) Investigation into the extractiona and application of routing time delays in Virtex-5 FPGAs. Invited by Prof. Peter Athanas.